UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. |
|---|---|---|---|
| 09/785,006 | 02/16/01 | SCHOENFELD A | 303.259US3 |

MM21/0925
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P
P.O. BOX 2938
MINNEAPOLIS MN 55402

| EXAMINER | |
|---|---|
| PERT, E | |
| ART UNIT | PAPER NUMBER |
| 2813 | |

DATE MAILED: 09/25/01

**Please find below and/or attached an Office communication concerning this application or proceeding.**

**Commissioner of Patents and Trademarks**

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/785,006 | SCHOENFELD, AARON | |
| | Examiner | Art Unit | |
| | Evan T. Pert | 2813 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Peri d f r Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *11-25 and 35-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-25 and 35-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Election/Restrictions*

1. Applicant's election without traverse of claims 11-25 in Paper No. 6 is acknowledged. Claims 26-34 were cancelled, while claims 35-43 were added, leaving claims 11-25 and 35-43 pending.

### *Information Disclosure Statement*

2. The examiner acknowledges applicant's submission of a 1449 in paper no. 3, but this form was seemingly not located in the file wrapper at the time of examination. Accordingly, the examiner suggests that applicant provide an additional copy of the Form 1449 originally filed with paper no. 3, with the response to this Office Action.

### *Claim Rejections - 35 USC § 112*

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 11-25 and 35-43 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

- The meaning of "perimeter edge" 18 as compared to "planar edge" is not defined by the specification, leaving the meaning of both unclear in all of the pending claims. For example, when considering a well-known prior art chip, a single "planar edge" can be thought of as the vertical *wall* between the top and bottom of the chip, while this very "planar edge" can be considered as being bounded by 2 "*perimeter* edges" that are the *lines* were the "planar edge" meets the top and the bottom of the chip, respectively.

In view of the lack of clarity, the examiner properly interprets the "edges" in the claims with a broadest reasonable interpretation in view of terms known in the prior art.

- In claim 22, line 6, the "*means* for providing" is not understood as all chips with edges have such a "means" which is the edge itself.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 11, 13 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by either Mori et al. OR Badehi.

Both Mori et al. and Badehi teach a rectangular chip (die) that has a first planar surface with circuitry and a surface "opposite" where "opposite" does not even require "parallelism". Thus, in Badhei, applicant's "first planar surface" corresponds to the angled surface delineated by Ref 14, for example. In Mori et al., the perimeter edges being "lines" at the upper and lower surfaces, while the "planar edge" is the sidewall. Contact notches 33b can also be considered as having edges, so there is more than one "edge". Clearly, the surfaces are "treated" to form electrical contacts and to separate the chips from the wafer.

6. Claims 18-25, 35-37 and 40-43 are rejected under 35 U.S.C. 102(e) as being anticipated by Ishida. Ishida teaches a dicing method that results in chip configurations claimed by applicant. For example, comparing Figs. 1D and 2D, there are two parallel "planar edges" in 11 and 10 wherein both 11 and 10 form a "chip" or "die". Circuitry is in a plane above the interface of 10 and 11 (Col. 2, lines 37-39). Each planar edge is clearly "flat" and "smooth" as seen in the Figures.

7. Claims 22-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Mori et al.. Without repeating limitations discussed above, Mori teaches that the planar edges should be smooth and flat so they can be abutted against other chips [col. 3, lines 6-18].

***Claim Rejections - 35 USC § 103***

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 12 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over either Mori et al. OR Badehi as applied to claims 11 and 15 above, and further in view of Bean et al.. While Mori and Badehi are silent with respect to "polishing" of "die" edges, Bean et al. mentions this as a well known practice, while not necessarily a preferable practice due to possible damage, a prior art practice none-the-less [col. 2, lines 11-25].

It would have been obvious at the time of applicant's invention to have modified either Mori or Badehi et al. by polishing the edges as was well-known in the art as established by Bean et al.. One of ordinary skill in the art would have been motivated to polish the edges to obtain a smooth surface that can be abutted to another chip.

10. Claims 25 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida as applied to claims 25 and 35 above, and further in view of Bean et al.. The same arguments apply as in item 9 above, with respect to polishing edges.

11. Claims 14, 16 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishida, Mori et al. and/or Badehi, as applied to claims 11, 15 and 35 above, and further in view of Hart et al..

Mori et al., Ishida and Badehi are silent about "grinding" the edges of a semiconductor chip (die), but Hart et al. are not. Hart et al. teach an apparatus that is specifically designed to grind the edges of a rectangular semiconductor chip [Figs. 5 and 6 taken with col. 1, lines 49-53]. While Hart et al. are silent with respect to "why" this feature is provided, it is readily apparent that the machine is for "polishing" (title), and it is common knowledge that "polishing" can be thought of as very fine "grinding" and that "grinding" can be thought of as very coarse "polishing". This is analogous to using grades of sand paper switching from a coarse "grinding" to a fine "polishing".

It would have been obvious to grind (or polish) the edges of semiconductor chips (dice) as is shown in Fig. 5 of Hart et al.. One of ordinary skill in the art would have been motivated to grind at the suggestion of Hart et al. as a step prior to polishing in order to first "grind" the coarse striations from the cutting blade for a better "polish" in the same way someone would choose coarse grit sandpaper to grind a rough surface followed by fine grit sandpaper and polishing cloths to "polish". Smooth surfaces on the edges are desired so the polished/ground chip can be abutted against another chip, for example.

***Double Patenting***

12. Claims 11-25 and 35-43 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-16 of U.S. Patent No. 6,215,172. Although the conflicting claims are not identical, they are not patentably distinct from each other because the specification of each is identical and each provides full direction and teaching of the claims of the instant case.

13. Claims 11-25 and 35-43 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 8-10 of copending Application No. 09/785,006 (Published as US 2001/0004544 A1 on June 21, 2001). Although the conflicting claims are not identical, they are not patentably distinct from each other because the specification of the published application is identical to the instant application and the claims of the instant application are recognizable from the teachings and direction of the published application.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

***Conclusion***

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Evan T. Pert whose telephone number is 703-306-5689. The examiner can normally be reached on M-F (7:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Charles Bowers can be reached on 703-308-2417. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ETP
September 20, 2001

Charles Bowers
Supervisory Patent Examiner
Technology Center 2800